IN THE CLAIMS:

1. (original) An event edge synchronization system, comprising:

a first clock zone device configured to generate an event signal based upon a first clock rate;

a second clock zone device configured to operate at a second clock rate, which is asynchronous with said first clock rate; and

a synchronous notification subsystem configured to receive said event signal, synchronize said event signal to said second clock rate based upon an edge transition of said event signal and said second clock rate, and generate a synchronous notification signal therefrom.

2. (original) The event edge synchronization system as recited in Claim 1 wherein said synchronous notification subsystem further includes:

a first logic device configured to generate a first intermediate signal based upon said event signal and a clock signal of said second clock zone device;

a second logic device configured to generate a second intermediate signal based upon said first intermediate signal and said clock signal of said second clock zone device;

a third logic device configured to generate a third intermediate signal based upon said second intermediate signal and said clock signal of said second clock zone device; and

a comparison logic device configured to generate said synchronous notification signal based upon said second and third intermediate signals.

3. (original) The event edge synchronization system as recited in Claim 2 wherein said first, second and third logic devices are "D" type flip-flops.

4. (original) The event edge synchronization system as recited in Claim 2 wherein said comparison logic device is an exclusive-OR (XOR) gate.

5. (original) The event edge synchronization system as recited in Claim 1 wherein said synchronous notification subsystem synchronizes said event signal to said second clock rate based upon a positive edge transition of said event signal.

6. (original) A method of operating an event edge synchronization system, comprising:

generating an event signal based upon a first clock rate associated with a first clock zone device;

operating a second clock zone device at a second clock rate, which is asynchronous with said first clock rate;

receiving said event signal;

synchronizing said event signal to said second clock rate based upon an edge transition of said event signal and said second clock rate; and

generating a synchronous notification signal therefrom.

7. (original) The method as recited in Claim 6 wherein said synchronizing and generating further comprises:

generating a first intermediate signal based upon said event signal and a clock signal associated with said second clock rate;

generating a second intermediate signal based upon said first intermediate signal and said clock signal associated with said second clock rate;

generating a third intermediate signal based upon said second intermediate signal and said clock signal associated with said second clock rate; and

generating said synchronous notification signal based upon said second and third intermediate signals.

8. (original) The method as recited in Claim 7 wherein said generating said first, second and third intermediate signals further comprises employing "D" type flip-flops.

9. (original) The method as recited in Claim 7 wherein said generating said synchronous notification signal further comprises employing an exclusive-OR (XOR) gate.

10. (original) The method as recited in Claim 6 wherein said synchronizing is based upon a positive edge transition of said event signal.

11. (currently amended) An event edge synchronization system, comprising:

~~a first clock zone device~~ means that generates an event signal based upon a first clock rate;

~~a second clock zone device~~ means that operates at a second clock rate, which is asynchronous with said first clock rate; and

~~a synchronous~~ notification ~~subsystem~~ means that receives said event signal, synchronizes said event signal to said second clock rate based upon an edge transition of said event signal and said second clock rate, and generates a synchronous notification signal.

12. (currently amended) The event edge synchronization means as recited in Claim 11 wherein said ~~synchronous~~ notification ~~subsystem~~ means further includes:

~~a~~ first ~~logic device~~ means that generates a first intermediate signal based upon said event signal and a clock signal of said ~~second clock zone device~~ means that operates at a second clock rate;

a second ~~logic device~~ means that generates a second intermediate signal based upon said first intermediate signal and said clock signal of said ~~second clock zone device~~ means that operates at a second clock rate;

a third ~~logic device~~ means that generates a third intermediate signal based upon said second intermediate signal and said clock signal of said ~~second clock zone device~~ means that operates at a second clock rate; and

a comparison ~~logic device~~ means configured to generate said synchronous notification signal based upon said second and third intermediate signals.

13. (currently amended) The event edge synchronization means as recited in Claim 12 wherein said first, second and third ~~logic devices~~ means employ "D" type flip-flops.

14. (currently amended) The event edge synchronization means as recited in Claim 12 wherein said comparison ~~logic device~~ means employs an exclusive-OR (XOR) gate.

15. (currently amended) The event edge synchronization means as recited in Claim 11 wherein said ~~synchronous~~ notification ~~subsystem~~ means synchronizes said event signal to said second clock rate based upon a positive edge transition of said event signal.

16. (original) A fast pattern processor, comprising:

a data buffer that stores processing blocks associated with a protocol data unit (PDU);

a context memory subsystem associated with said data buffer that receives said processing blocks;

a pattern processing engine, associated with said context memory, that performs pattern matching upon said processing blocks; and

an output interface subsystem that receives said processing blocks from said data buffer or said context memory subsystem and re-transmits packets or payloads embodied within said processing blocks, said output interface subsystem, including:

a first-in-first-out (FIFO) buffer; and

an event edge synchronization system that provides a synchronous notification signal indicating that a block of data of said FIFO buffer has been retrieved and re-transmitted, said event edge synchronization system having:

a first clock zone device that generates an event signal based upon a first clock rate, said first clock zone device is associated with an output portion of said FIFO buffer;

a second clock zone device that receives said synchronous notification signal based upon a second clock rate and performs processing based upon said synchronous notification signal, said second clock rate asynchronous with said first clock rate; and

a synchronous notification subsystem that receives said event signal, synchronizes said event signal to said second clock rate based upon an edge transition of said event signal and said second clock rate, and generates said synchronous notification signal.

17. (original) The fast pattern processor as recited in Claim 16 wherein said synchronous notification subsystem further includes:

a first logic device that generates a first intermediate signal based upon said event signal and a clock signal of said second clock zone device;

a second logic device that generates a second intermediate signal based upon said first intermediate signal and said clock signal of said second clock zone device;

a third logic device that generates a third intermediate signal based upon said second intermediate signal and said clock signal of said second clock zone device; and

a comparison logic device that generates said synchronous notification signal based upon said second and third intermediate signals.

18. (original) The fast pattern processor as recited in Claim 17 wherein said first, second and third logic devices are "D" type flip-flops.

19. (original) The fast pattern processor as recited in Claim 17 wherein said comparison logic device is an exclusive-OR (XOR) gate.

20. (original) The fast pattern processor as recited in Claim 16 wherein said synchronous notification subsystem synchronizes said event signal to said second clock rate based upon a positive edge transition of said event signal.